Digit Serial Divider Area and Delay for the 5 NIST Polinomials
d express the amount of digit computed per clock cycle.

Table 1. Digit Serial Division for *m* = 571 in Virtex5.

d	cycles	FF	luts	period	delay (ns)	AxD
1	571	2873	2878	1,78	1016	2925,1
2	286	2873	6298	2,24	641	4034,8
3	191	2873	6891	2,74	523	3606,3
4	143	2875	10326	3,28	469	4843,3
5	115	2873	10901	3,89	447	4876,6
6	96	2874	15152	4,42	424	6429,3
8	72	2873	17831	5,56	400	7138,1

Table 2. Digit Serial Division for *m* = 409 in Virtex5.

d	cycles	FF	Luts	period	delay (ns)	AxD
1	409	2063	2068	1.78	728	1505.5
2	205	2063	4520	2.24	459	2075.6
3	137	2063	4947	2.46	337	1667.2
4	103	2065	7403	3.34	344	2546.8
5	82	2063	8437	3.65	299	2525.2
6	69	2063	10275	4.33	299	3069.9
7	59	2065	10698	4.73	279	2985.5
8	52	2063	12740	5.39	280	3570.8
9	46	2065	13585	6.05	278	3780.7

Table 3. Digit Serial Division for *m* = 283 in Virtex5.

d	cycles	FF	luts	period	delay (ns)	AxD
1	283	1433	1438	1.78	504	724.4
2	142	1433	3128	2.02	287	897.2
3	95	1432	3434	2.74	260	893.9
4	71	1432	5132	3.37	239	1227.9
5	57	1432	5424	3.93	224	1215.0
6	48	1435	7130	4.25	204	1454.5
7	41	1434	7447	4.91	201	1499.2
8	36	1436	8839	5.36	193	1705.6
9	32	1435	9961	6.13	196	1953.9

Table 4. Digit Serial Division for *m* = 233 in Virtex5.

d	cycles	FF	luts	period	delay (ns)	AxD
1	233	1182	1187	1.78	415	492.3
2	117	1183	2583	2.01	235	607.4
3	78	1182	2833	2.44	190	539.2
4	59	1183	4234	3.34	197	834.4
5	47	1182	4828	3.65	172	828.2
6	39	1183	5869	4.43	173	1014.0
7	34	1182	6123	4.69	159	976.4
8	30	1182	7284	5.39	162	1177.8
9	26	1185	7777	6.05	157	1223.3

Table 5. Digit Serial Division for *m* = 163 in Virtex5.

d	cycles	FF	luts	period	delay (ns)	AxD
1	163	832	836	1.73	282	234.6
2	82	832	1492	2.05	168	250.8
3	55	831	1992	2.73	150	299.1
4	41	833	2968	3.36	138	408.9
5	33	832	3161	3.73	123	389.1
6	28	834	4116	4.28	120	493.3
7	24	831	4321	4.75	114	492.6
8	21	834	5128	5.45	114	586.9
9	19	833	5784	5.89	112	647.3