Practical work nº 0 (tutorial) - Introduction to VHDL and ModelSim

1 Goals

Generate VHDL models of combinational circuits and simulate them with ModelSim. We will use the Xilinx ISE (Integrated Software Environment) to edit the files.

2 Previous work

2.1 Generate a VHDL model of the circuit of figure 1.

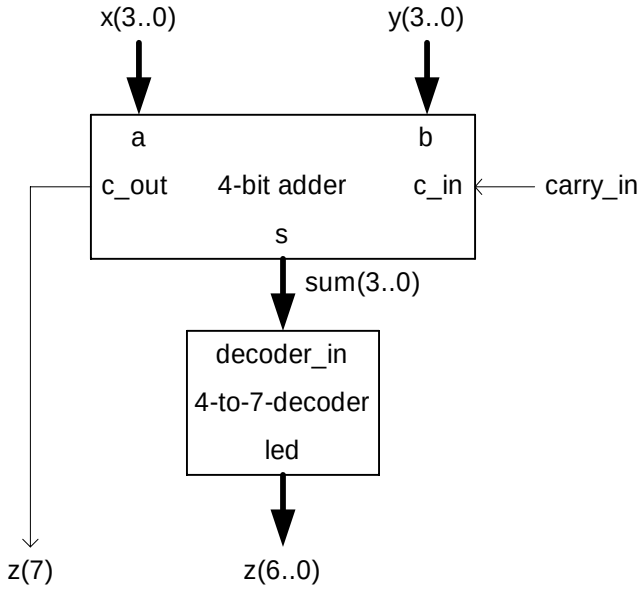

Figure 1 Adder and 4-to-7 decoder

For modeling the adder use either the iterative construction of sections 8 and 9, or the direct sum definition of section 10. Two models of a 4-to-7 decoder are given in section 7.

2.2 Save the model as *practi0.vhd*.

2.3 Compute the value of *z* for the following combinations of input values:

x = 1001	*y* = 0111	*carry_in* = 1
x = 1101	*y* = 0101	*carry_in* = 1
x = 0001	*y* = 1111	*carry_in* = 0
x = 0101	*y* = 0110	*carry_in* = 0

3 Practical work

Using the ISE environment.

3.1 Create a project: (file -> create project…)
- Select a name for the project and a directory to store the files (ej: pract0 and d:\curso\pract0)
- Select a Spartan 3 device with a pq208 package
- Simulator: ISE/Simulator; Prerrefered language: vhdl
- Then finish the wizard.

3.2 create file or add file to the project (3.2a or 3.2b)

3.2a. add an existing file
Project -> add source…

Select the desired source file (*practi0.vhd*)

3.2b. create file:
Project -> new source, select VHDL module; file name: ejer0. Pres “next”
Define the ports. Inputs: X(3:0), Y(3:0) and carry_in, and outputs: z(7:0). . Pres “next”
Type the desired code into the *arquitecture* region, between the “*begin*” and “*end behavioral*” keywords.

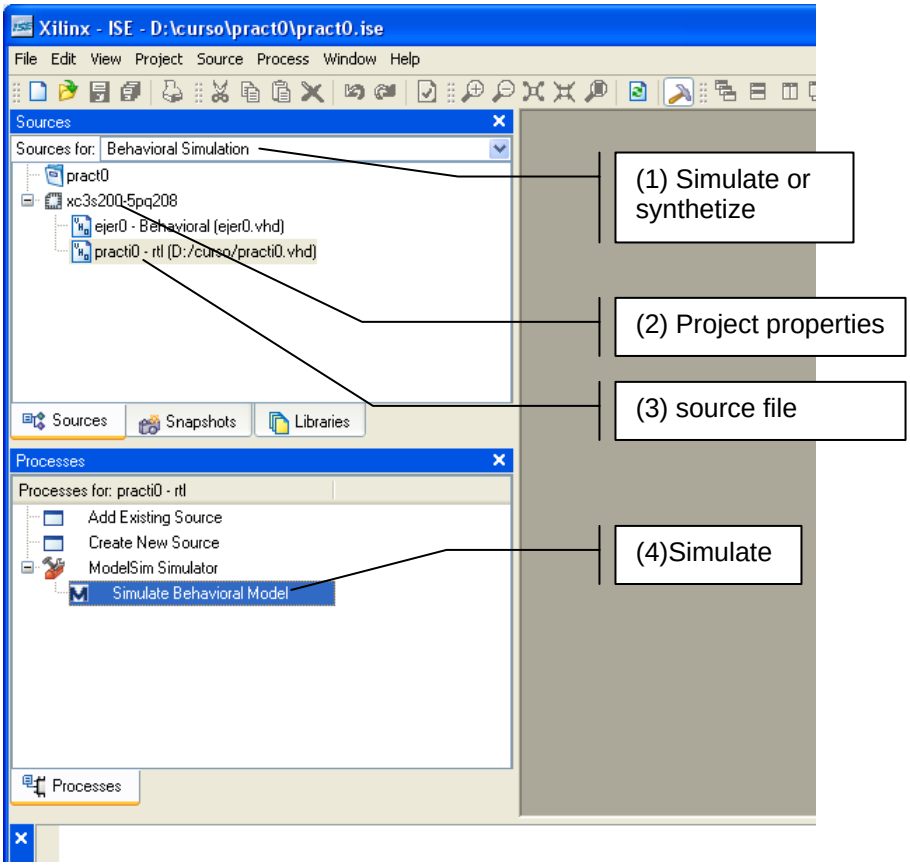

Figure 1. ISE environment.

3.3 Simulate the design:

We will explore three different possibilities to simulate our simple design.
- ISE simulator
- Modelsim and add stimuli
- Create a testbech web form and simulate

3.4 Simulate with ISE simulator

3.4.1 Ensure that:
- In “project properties” (right button on (2) of figure 1) simulate = ISE simulator
- In “Source for”, ensure to select Behavioral Simulation (see (1) in figure 1).
- Select the soured file to simulate (3)

3.4.2 Double click in “simulate behavioral model”. It will open the ISE simulator.

3.4.3 In console window input stimuli:

```
put x 1001
put y 0111
put carry_in 1
run 200
put y 0101
run 200
etc.
```

3.4.4 Check the simulation results (compare with the foreseen values of *z*).

3.5 Simulate with Modelsim

3.5.1 Ensure that:
- In “project properties” (right button on (2) of figure 1) simulate = Modelsim XE - VHDL
- In “Source for”, ensure to select Behavioral Simulation (see (1) in figure 1).
- Select the soured file to simulate (3)

3.5.2 Double click in simulate behavioral model. It will open modelsim application (a separate program).

3.5.3 In modelsim transcript window input stimuli (see 2.3):

```
force x 1001
force y 0111
force carry_in 1
run 200
force x 1101
force y 0101
force carry_in 1
run 200
etc.
```

The previous commands can be

inputted at the command line (interactive simulation),

previously edited (File / New / Source / Do), saved within the working directory as (for example) *practi0.do*, added to the working space (File / Add to Project / Existing File) and executed from the command line: `do practi0.do` (batch simulation).

3.5.4 Execute the do file.

3.5.5 Change some view and wave options options

3.5.6 Check the simulation results (compare with the foreseen values of *z*).

3.6 Simulate with a simple testbench (test bench waveform)

3.6.1 Create a Test Bench WaveForm.
- Project -> new source
- Select test bench WaveForm and give a name like “test_pract0.tbw
- In the next window select the file which to associate to the new Test Bench.
- In Initial timing and clock wizard select combinatorial.

3.6.2 Design the test bench
- Add some stimuli to the wave form.
- save the file

3.6.3 Double click in simulate behavioral model. It will open modelsim application (a separate program).

3.6.4 Check the simulation results (compare with the foreseen values of *z*).