Practical work nº 2 - Registers and counters

1 Goals

Generation of VHDL models of sequential circuits.

2 Previous work

2.1 Generate the VHDL model of an *n*-bit up-down counter, with asynchronous *reset*, *count* enable input and *upb_done* control input: if *upb_down* = 0, count up, and if *upb_down* = 1, count down (figure 1):

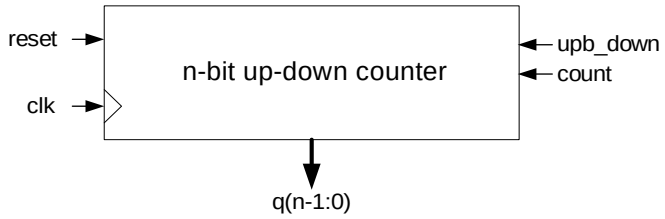

Figure 1 Up/down counter

2.2 Generate the VHDL model of a bi-directional *n*-bit shift register (figure 2). Its working is defined by the value of a 2-bit *control* signal:

if *control* = 01, the *parallel* input is loaded within the register;
if *control* = 10, the register contents is shifted one position to the left and the new less significant bit is *serial_low*;
if *control* = 11, the register contents is shifted one position to the right and the new less significant bit is *serial_high*;
if *control* = 00, the register contents is not modified.

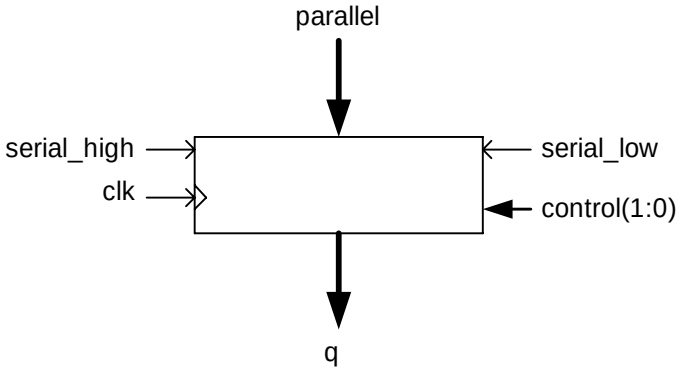

Figure 2 Bi-directional shift register (symbol)

It can be modeled according to the scheme of figure 3.

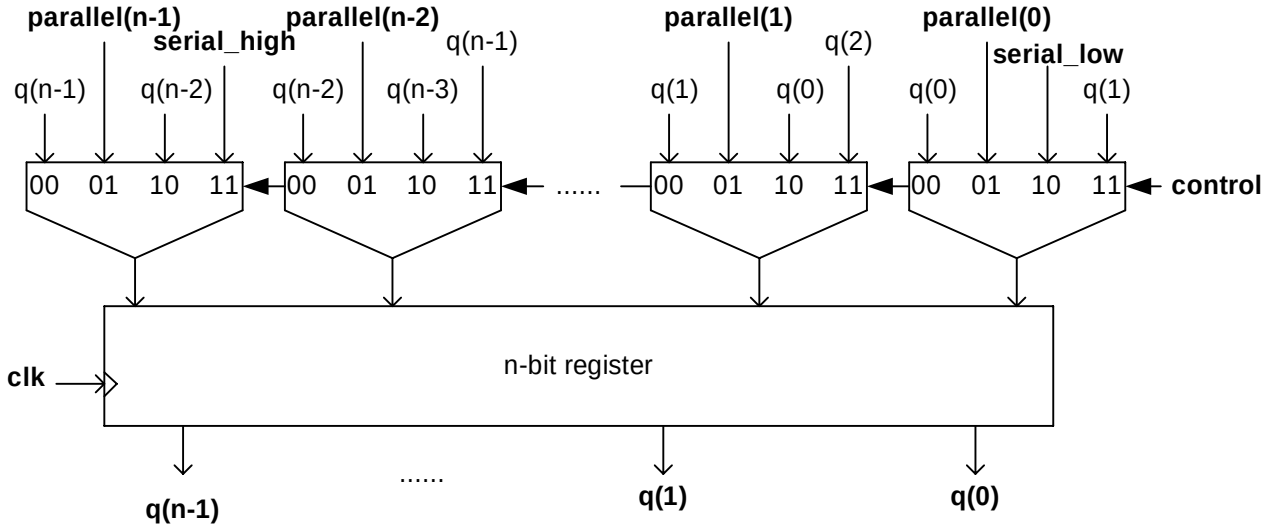

Figure 3 Bi-directional shift register (circuit model)

2.3 Generate command files (.do) for both circuits.

3 Practical work

3.1 Simulation of both circuits. One generating a command file, and another using a test bench wave form. Try to test all the characteristics.
3.2 (optional) add to circuit of 2.2 an enable signal, both serial out (serial_high_out, serial_low_out) and asynchronous reset like in figure 4.
3.3 (optional) generate an exhaustive VHDL test bench for one of the previous designs.

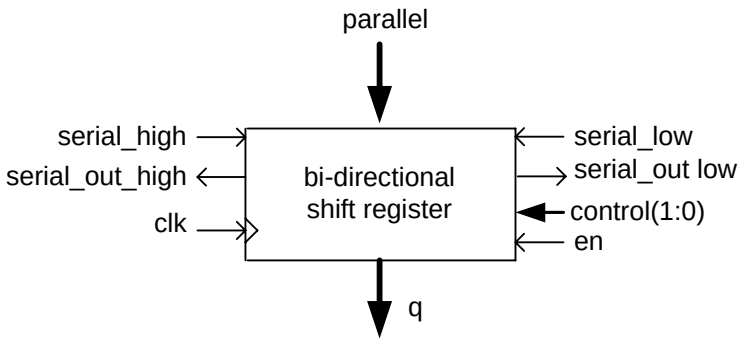

Figure 4 Bi-directional shift register with serial in and out