1 Specification

The system to be developed uses the PicoBlaze virtual processor as a main component. The system will functions for the Digilent Spartan-3 development board described and used in lab4. The inputs are three buttons and the eight switches available in the board. They will be used to input a 32 bit number X. The system will calculate:

$z = x \bmod 239$

In order to compute the modulo operation the divisor described in lab1 should be used as coprocessor. As output the system will display the result into the four seven-segment available in the board. The student should decide how to input the data.

2 Hardware platform

The fast-prototyping board Digilent Spartan-3 development board (www.digilentinc.com) will be used.

3 Hardware – software partitioning

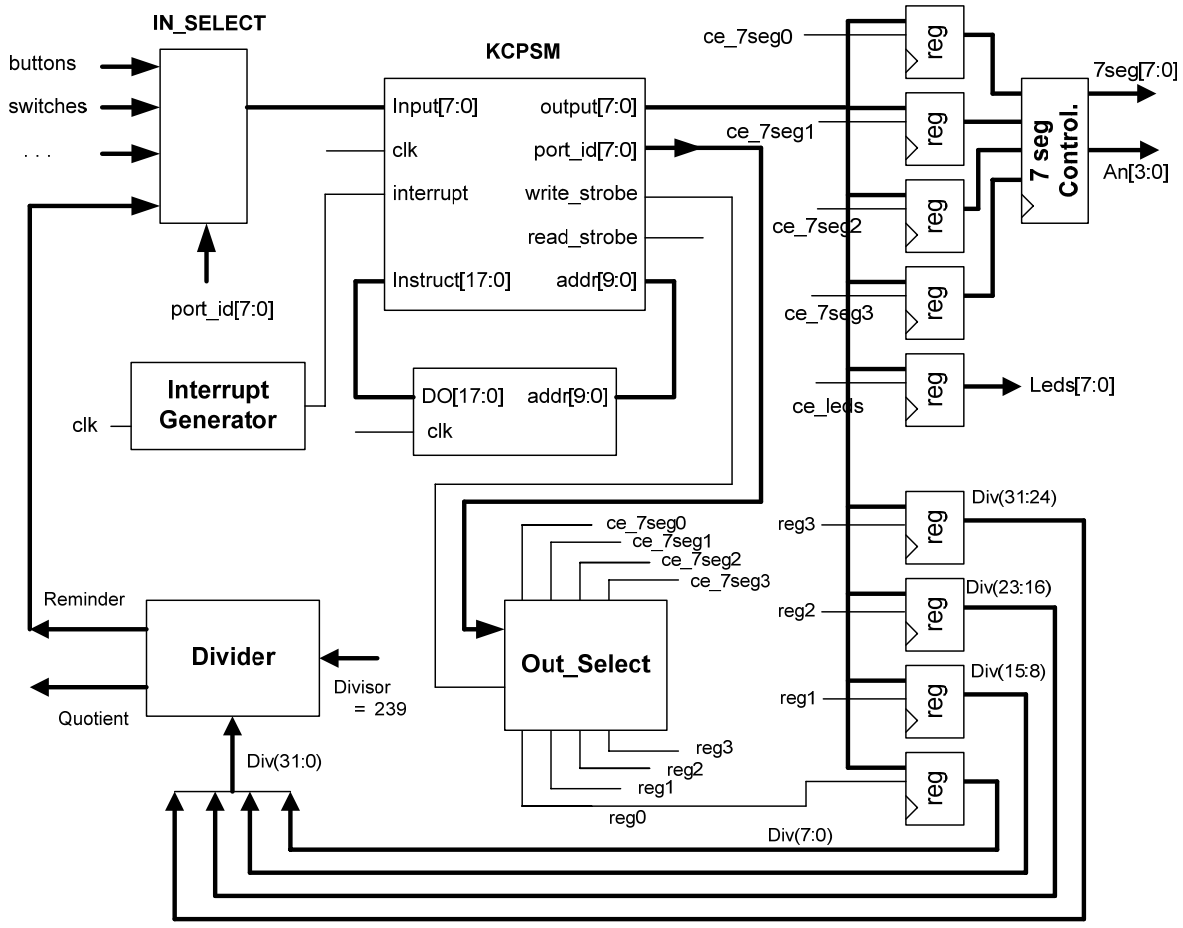

Figure 1 Block diagram

The proposed block diagram is shown in figure 1. The processor is in charge of reading the four bytes that makes the dividend. Then output the operand to the coprocessor (*x*(31:24), *x*(23:16), *x*(15:0), *x*(7:0)). Four 8-bit registers holds the 32 bit dividend for the divider. The divisor is the constant 239. The Quotient is discarded and the reminder of a 32 by 8 bits divider gives the expected result.

4 Program generation (software)

Use *pBlaze IDE version: 3.7.4 ß* (a free assembler for PicoBlaze) for generate the equivalent assembly language program and simulate its execution.

5 Complete system modeling and simulation

Generate a VHDL model of the circuit of figure 1, for example *main.vhd*. For that, you can start with the project of lab4.
You need to add to this project:

- A divider: use a previously defined divider form lab1.
- Modify the *out_select* logic in order to generate enable signals for the 4 registers that holds the dividend.
- Add the 4 register that holds the dividend. Remember to use the enable signals generated in *out_select*
- Modify the *in_select* logic in order to enable the possibility to input the result of divisor. That is add an input to the multiplexer and connect to the reminder output of divisor.

Simulate using modelsim the functionally of the whole system.

6 Synthesis, implementation and downloading the design.

Use the programs XST (Xilinx Synthesis Technology) and ISE (Integrated System Environment), available within *Xilinx – Project Navigator*.

Before, define the assignment of FPGA pins to the circuit signals in the same fashion of lab4.

Program the board using the JTAG cable and test the circuit.